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| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date : Thu Oct 17 09:48:56 2024

| Host : Samuel running 64-bit major release (build 9200)

| Command : report\_power -file hello\_world\_arty\_a7\_power\_routed.rpt -pb hello\_world\_arty\_a7\_power\_summary\_routed.pb -rpx hello\_world\_arty\_a7\_power\_routed.rpx

| Design : hello\_world\_arty\_a7

| Device : xc7a100ticsg324-1L

| Design State : routed

| Grade : industrial

| Process : typical

| Characterization : Production

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Power Report

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1. Summary

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| Total On-Chip Power (W) | 0.080 |

| Design Power Budget (W) | Unspecified\* |

| Power Budget Margin (W) | NA |

| Dynamic (W) | 0.009 |

| Device Static (W) | 0.071 |

| Effective TJA (C/W) | 4.6 |

| Max Ambient (C) | 99.6 |

| Junction Temperature (C) | 25.4 |

| Confidence Level | Medium |

| Setting File | --- |

| Simulation Activity File | --- |

| Design Nets Matched | NA |

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\* Specify Design Power Budget using, set\_operating\_conditions -design\_power\_budget <value in Watts>

1.1 On-Chip Components

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| On-Chip | Power (W) | Used | Available | Utilization (%) |

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| Clocks | 0.003 | 4 | --- | --- |

| Slice Logic | 0.002 | 4916 | --- | --- |

| LUT as Logic | 0.002 | 2394 | 63400 | 3.78 |

| CARRY4 | <0.001 | 158 | 15850 | 1.00 |

| Register | <0.001 | 1768 | 126800 | 1.39 |

| F7/F8 Muxes | <0.001 | 339 | 63400 | 0.53 |

| Others | 0.000 | 15 | --- | --- |

| Signals | 0.003 | 3871 | --- | --- |

| Block RAM | 0.002 | 2 | 135 | 1.48 |

| I/O | <0.001 | 3 | 210 | 1.43 |

| Static Power | 0.071 | | | |

| Total | 0.080 | | | |

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1.2 Power Supply Summary

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| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) |

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| Vccint | 0.950 | 0.019 | 0.010 | 0.009 |

| Vccaux | 1.800 | 0.016 | 0.000 | 0.016 |

| Vcco33 | 3.300 | 0.000 | 0.000 | 0.000 |

| Vcco25 | 2.500 | 0.000 | 0.000 | 0.000 |

| Vcco18 | 1.800 | 0.000 | 0.000 | 0.000 |

| Vcco15 | 1.500 | 0.000 | 0.000 | 0.000 |

| Vcco135 | 1.350 | 0.000 | 0.000 | 0.000 |

| Vcco12 | 1.200 | 0.000 | 0.000 | 0.000 |

| Vccaux\_io | 1.800 | 0.000 | 0.000 | 0.000 |

| Vccbram | 0.950 | 0.000 | 0.000 | 0.000 |

| MGTAVcc | 1.000 | 0.000 | 0.000 | 0.000 |

| MGTAVtt | 1.200 | 0.000 | 0.000 | 0.000 |

| Vccadc | 1.800 | 0.018 | 0.000 | 0.018 |

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1.3 Confidence Level

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| User Input Data | Confidence | Details | Action |

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| Design implementation state | High | Design is routed | |

| Clock nodes activity | High | User specified more than 95% of clocks | |

| I/O nodes activity | Medium | More than 5% of inputs are missing user specification | Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view |

| Internal nodes activity | Medium | User specified less than 25% of internal nodes | Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views |

| Device models | High | Device models are Production | |

| | | | |

| Overall confidence level | Medium | | |

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2. Settings

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2.1 Environment

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| Ambient Temp (C) | 25.0 |

| ThetaJA (C/W) | 4.6 |

| Airflow (LFM) | 250 |

| Heat Sink | medium (Medium Profile) |

| ThetaSA (C/W) | 4.6 |

| Board Selection | medium (10"x10") |

| # of Board Layers | 12to15 (12 to 15 Layers) |

| Board Temperature (C) | 25.0 |

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2.2 Clock Constraints

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| Clock | Domain | Constraint (ns) |

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| clkdiv2 | clock\_50mhz | 20.0 |

| clock | clock | 10.0 |

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3. Detailed Reports

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3.1 By Hierarchy

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| Name | Power (W) |

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| hello\_world\_arty\_a7 | 0.009 |

| rvsteel\_mcu\_instance | 0.009 |

| rvsteel\_core\_instance | 0.006 |

| rvsteel\_ram\_instance | 0.002 |

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